In the Specification:

Please replace the paragraph beginning on page 16, line 30 with the following (The changes made to this paragraph in the Amendment filed on October 29, 2004, have been incorporated without being marked-up):

The first sampled value Y_t and the second sampled value Y_{t-1} set in the FF 331 are input to the subtracter 333, which subtracts Y_{t-1} from Y_t to calculate a first difference. At the same time, the second sampled value Y_{t-1} set in the FF 331 and the third sampled value Y_{t-2} set in the FF 332 are input to the subtracter 334, which subtracts Y_{t-2} from Y_{t-1} to calculate another first difference. The first difference calculated by the subtracter 333 is output to the code determination circuit 335. The code determination circuit 335 determines the ternary code for the first difference calculated by the subtracter 333, or determines $hat_{t, t-1}$, and outputs $hat_{t, t-1}$ to the multiplier 337. Simultaneously, the first difference calculated by the subtracter 334 is output to the code determination circuit 336. The code determination circuit 336 determines the ternary code for the first difference calculated by the subtracter 334, or determines $hat_{t-1, t-2}$, and outputs $hat_{t-1, t-2}$ to the multiplier 338. The product of Y_t-Yt-$_1$ ~~and $hat_{t-1, t-2}$~~ $\underline{hat_{t, hat\ t-1}}$ calculated by the multiplier 337 and the product of Y_{t-1}-Y_{t-2} and ~~$hat_{t, t-1}$~~ $\underline{hat_{t-1, t-2}}$ calculated by the multiplier 338 are output to the subtracter 339. The subtracter 339 finally determines the phase error of the clock signal from the above equation. In other words, the subtracter 339 uses the absolute values of the two first differences, which are calculated by multiplying each of the two first differences by the ternary code "hat" to correct the transition direction, so as to calculate the difference between the two absolute values

from the above equation (a second difference), which is equal to the phase error of the clock signal.